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Enhanced resolution and high aspect-ratio semiconductor nanopatterning by metal overcoating

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We present a focused ion beam semiconductor nanopatterning technique enabling high resolution and high-aspect ratios. Undesired semiconductor material removal due to residual lower-intensity ion beam tails is prevented by a 20 nm slow-etch-rate TiO_2 layer acting as an effective saturated-absorber dynamic mask. Resulting semiconductor features smaller than 30 nm and deeper than 350 nm correspond to aspect ratio higher than 10, while for larger features the aspect ratio can be as high as 15. The experimentally demonstrated results are in good agreement with the theoretical predictions. A transmission spectrum of a microcavity realized by this method conforms to numerical calculation results. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3080207]

Focused ion beam (FIB) etching is widely used as a versatile maskless lithography technique in numerous fields. The trend of patterning smaller structures, within the nanoregime, necessitates the nanometer-scale control of the ion-induced material modifications. Nanopatterning using FIB etching is generally employed to develop or locally modify devices, including integrated circuits, microsystems, and microphotonics. Many photonic and optoelectronic devices employ subwavelength-scale structures, such as diffraction gratings, distributed Bragg reflectors (DBRs), photonic crystals[1–4] for high performance laser diodes,[5] semiconductor nonlinear optics,[6] and surface-plasmon devices.[7] These nanostructures cannot be fabricated using conventional contact photolithography and thus nanoscale patterning techniques such as electron-beam lithography and FIB patterning are necessary.

Due to the merit of FIB patterning, namely, being a single-step rapid process; however, with small throughput, it is mainly exploited in the course of developing prototypes of both electrical and optical devices.[8] High aspect-ratio patterning is becoming essential and some progress has been achieved, e.g., deep nanopatterns in diamondlike materials with aspect ratios higher than 20.[9] However, in semiconductors commonly used in microelectronics and integrated photonics, high aspect-ratio nanoscale milling cannot be achieved due to the material fast sputter rates in the beam tail regions,[10] and thus deep FIB milling in semiconductors was reported only for feature sizes larger than 0.15 μm.[11] Polymer protective layers thicker than 0.2 μm were shown to improve FIB milling in semiconductors;[12] however, they require spin coating techniques not applicable to local device modifications and are applicable only for features larger than 0.5 μm.

Here we demonstrate a technique allowing the fabrication of high aspect-ratio nanoscale semiconductor structures and local device modifications using FIB technology. The unwanted semiconductor sputtering in the exterior part of the ion beam due to the tail ion concentration is prevented by a thin oxidized Ti layer TiO_2, which has very slow sputter rate (<0.15 $\mu m^3/nCb$); thus acting as a saturated-absorber dynamic mask for the semiconductor. When the central region of the TiO_2 mask is etched, the exposed semiconductor is being milled rapidly while the lower flux beam edges are stopped by the still existing TiO_2 mask. Unlike the polymer protective-layer techniques, the metal-oxide protective layer can be deposited locally within the FIB, thus enabling this technique for local device modifications. Furthermore, metal protective layers allow much higher resolution, and nanoscale milling is achieved with very high aspect ratios as will be discussed here. The sputtering rate selectivity between the semiconductor and the oxidized metallic protective layers determines the minimal feature size of the created dynamic mask. Using ion- or electron-assisted deposition within FIB is a commonly used technique for creating a protective layer before making a cross section. Ion-assisted deposition is much faster than the electron-assisted one, while electron beam-induced deposition offers the advantage of not sputtering the deposited material or implanting gallium simultaneously. For this purpose, the multiple gas injection system is installed on most FIB systems, allowing the deposition of metals or dielectrics (most frequently Pt or C) locally on the sample. This technique can deposit the protective mask with a material with slow sputtering rate before etching the nanostructures within the same FIB session.

In order to calculate the exact milling profile dependence on the material properties, the following model was employed. Assuming linear dependence of the milling rate on ion beam intensity, the milled profile depth recursive time dependence is

$$z(x,t) = z(x,0) + z(x,t-\Delta t)\cdot R[z(x,t-\Delta t)], \quad (1)$$

where $R[z]$ is the milling rate z-dependence for a given layer structure, x is the lateral dimension, and Δt is the time step used in numerical calculations. Numerical calculations were performed for GaAs milling with TiO_2 protective layers of various thicknesses [Fig. 1(c)] with ~20 nm FIB beam diameter. According to the calculations for well-separated features, the milling aspect ratio is higher with the TiO_2 layer [Fig. 1(c), solid blue] than that of a bare semiconductor milling (Fig. 1, dashed red) for the minimal ion beam diameter available in practical systems.

Our milling experiments were conducted with a Ga^+ liquid metal ion source in the FEI Strata 400 FIB system. The

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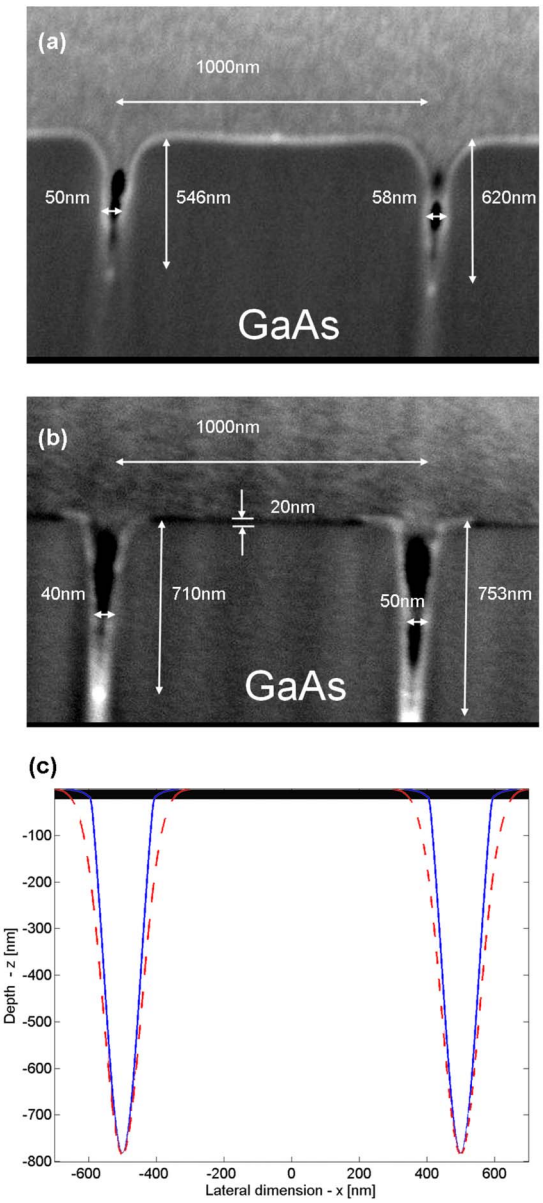

FIG. 1. (Color online) Scanning electron microscopy (SEM) cross-section image of milling depth profile for well-separated features ~50 nm wide with different ion doses (a) bare GaAs sample and (b) 20 nm TiO_2 coated GaAs sample. (c) Calculated profiles for similar depth for bare sample (dashed red) and TiO_2 coated one (solid blue).

system was operated at an acceleration voltage of 30 kV with a beam dwell time of 1 μs, a 50% overlap, and a beam current of 28 pA, corresponding to a beam diameter of 50 nm. The milling experiments were performed on a GaAs substrate and all the features are several microns long trenches. GaAs-based materials have been shown to have very fast FIB sputter rates $>0.61\ \mu m^3/nCb$.[5] A protective TiO_2 layer appeared to improve the aspect ratio of the well-separated millings [Figs. 1(a) and 1(b)].

Applying the protective layer appears to have an even stronger effect on improving the resolution of closely located features. According to the calculations [Fig. 2(c)] for ~100 nm features with ~200 nm separation, the sample coated by a protective layer remains intact, while the bare GaAs is unable to maintain the designed pattern. The experimental milling of the closely located feature pattern shows better structure shape for the coated sample at large separations between features. Moreover, at separations of ~200 nm, the 100 nm millings virtually merge in the bare semiconductors sample, while for similar conditions, a perfect structure is maintained on the coated sample [Figs. 2(a) and 2(b)].

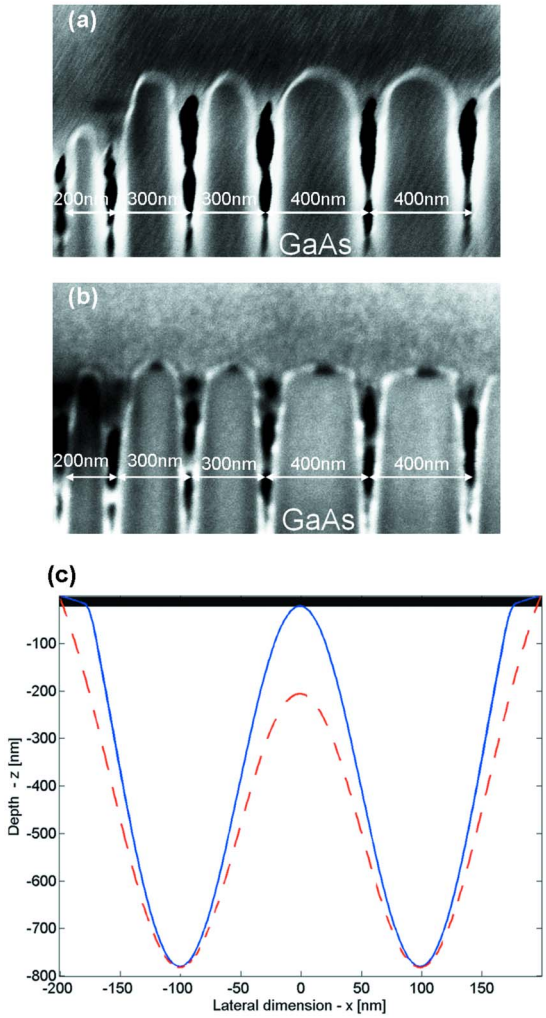

FIG. 2. (Color online) SEM cross-section image of milling depth profile for ~50 nm wide features with various separations (a) bare GaAs sample (b) 20 nm TiO_2 coated GaAs sample. (c) Calculated profiles for similar depth for bare sample (dashed red) and TiO_2 coated one (solid blue).

As the features are made even smaller, the enhancement in resolution due to the protective layer becomes more significant. The theoretical model predicts unintentional overetching of the bare material between the trenches, which is however prevented by the protective TiO_2 layer [Fig. 2(c)]. For finer feature milling, the FIB current was set to 11 pA corresponding to the beam diameter of 10 nm. The samples consisted of bare $Ga_{0.45}In_{0.55}P$ and $(Al_{0.5}Ga_{0.5})_{0.51}In_{0.49}P$ layers epitaxially grown on a GaAs and similar structures coated with protective TiO_2 layers. Only the $(Al_{0.5}Ga_{0.5})_{0.51}In_{0.49}P$ top layer was milled. The sample contained also $Ga_{0.45}In_{0.55}P$ quantum well layers about 500 nm below the surface. The ~350 nm deep milling is still well above the quantum well region. The patterning resolution in our experiments allowed the preparation of small features of 30 nm with very high aspect ratio >10, while the bare semiconductor milling did not allow aspect ratios more than 3.5 (Fig. 3) and, in addition, a noticeable deterioration of the top semiconductor layer.

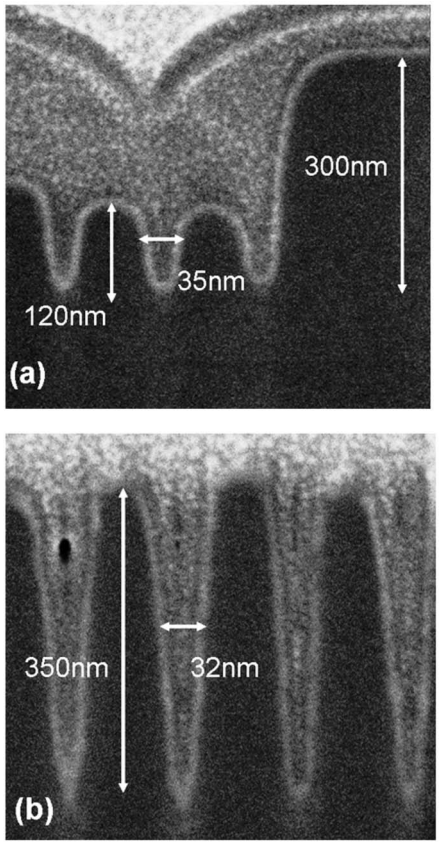

FIG. 3. SEM cross-section image ~30 nm features (a) – bare semiconductor sample. (b) −20 nm TiO_2 coated semiconductor sample.

Different milling conditions were studied for bare semiconductor samples and for samples coated by 10 and 20 nm TiO_2 layers. Increasing the ion dose resulted in deeper milling; however, it was limited by the damage done to the protective TiO_2 layer. Thicker TiO_2 layer was able to withstand longer milling times and thus larger depths could be achieved. Nonetheless, even for a very thick TiO_2 layer, which remained intact during a very long milling time, the depth exhibited saturation caused by the material redeposition, which becomes dominant at very high aspect ratios, and thus an optimal TiO_2 thickness was concluded to be about 20 nm in order to achieve the maximal depth under these ion beam conditions. In principle, redepositon effect may be reduced by employing multipass milling techniques suitable for specific milling profiles. Using a 20 nm TiO_2 layer with 10 nm ion beam diameter and an ion dose of ~5 $n\mathrm{Cb}/\mu\mathrm{m}^2$ yielded ~30 nm size features with 350 nm depth [Fig. 3(b)] corresponding to an aspect ratio higher than 10.

Realization of semiconductor microcavities is complicated and implementations based on DBRs require high coupling constant of the grating with the field modes, usually located deep below the surface, making a high aspect ratio of grating features a crucial factor in the fabrication. The developed method was applied for the fast throughput realization of a challenging photonic device—an integrated microcavity by periodic FIB milled structures on a 4 μm wide by 0.4 μm high ridge waveguide etched on $(Al_{0.5}Ga_{0.5})_{0.51}In_{0.49}P$ grown on GaAs (inset of Fig. 4). The 10 μm long microcavity was designed to have a resonance at 1512 nm, using three-dimensional finite difference time

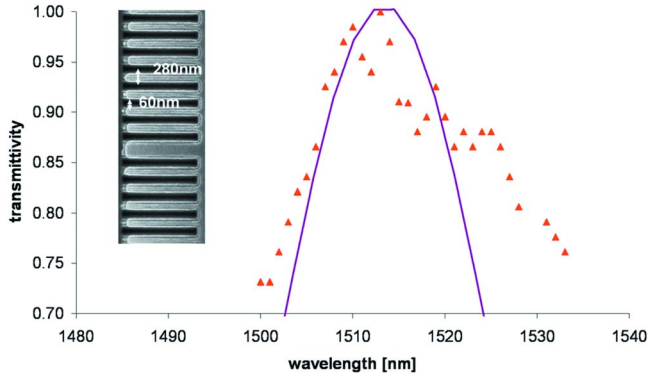

FIG. 4. (Color online) Transmission spectrum of a microcavity based on deep FIB milled gratings experimental (triangles) and calculated (solid line). The inset is a SEM image of the microcavity.

domain simulations. The optical measurements were performed by a tunable telecom wavelength laser (1500–1535 nm), which was facet coupled into the waveguide with about 2 μm^2 mode area by a lensed fiber. The measured microcavity transmission spectrum (Fig. 4) exhibits a resonant maximum near 1512 nm in good agreement with simulations; however, the experimental transmission spectrum is slightly wider than the calculated one due to the fabrication imperfections such as milling depth and width variations.

In conclusion, we have demonstrated a high aspect-ratio FIB milling technique, which presents a generic method for deep nanopatterning in semiconductors with high resolution. A protective 20 nm TiO_2 layer significantly improved the GaAs-based material patterning resolution in our experiments allowing very high-aspect ratio features as small as 30 nm with more than 350 nm depth. For larger features of ~100 nm, aspect ratios as high as 15 were achieved. This method was shown to generate nanoscale subwavelength-feature photonic structures such as DBRs and gratings and microcavities for the developing field of short-wavelength photonics and nonlinear optics.[13] Moreover, it could provide the essential solution for silicon debug and repair considering the continued shrinking of device dimensions in Si very large scale integrated circuits, enabling probing at a single device level.

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